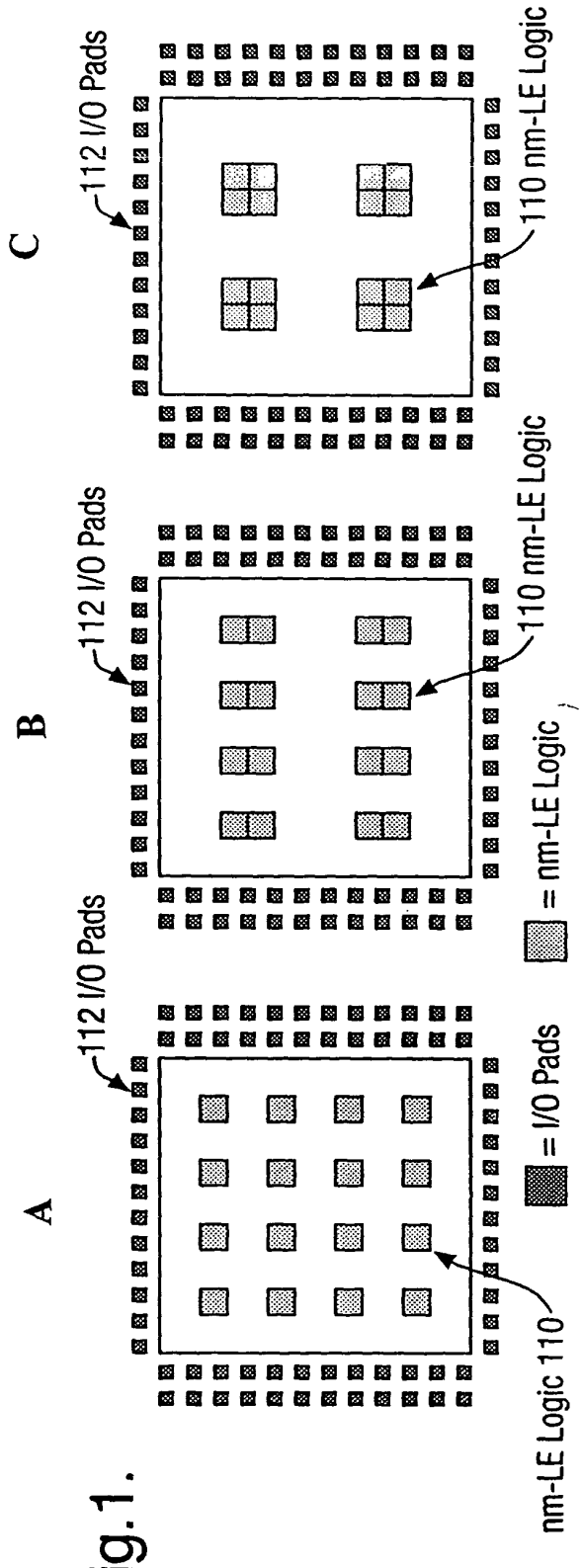

A
B
C
112 I/O Pads
110 nm-LE Logic
nm-LE Logic 110
= I/O Pads
= nm-LE Logic

Fig. 1.

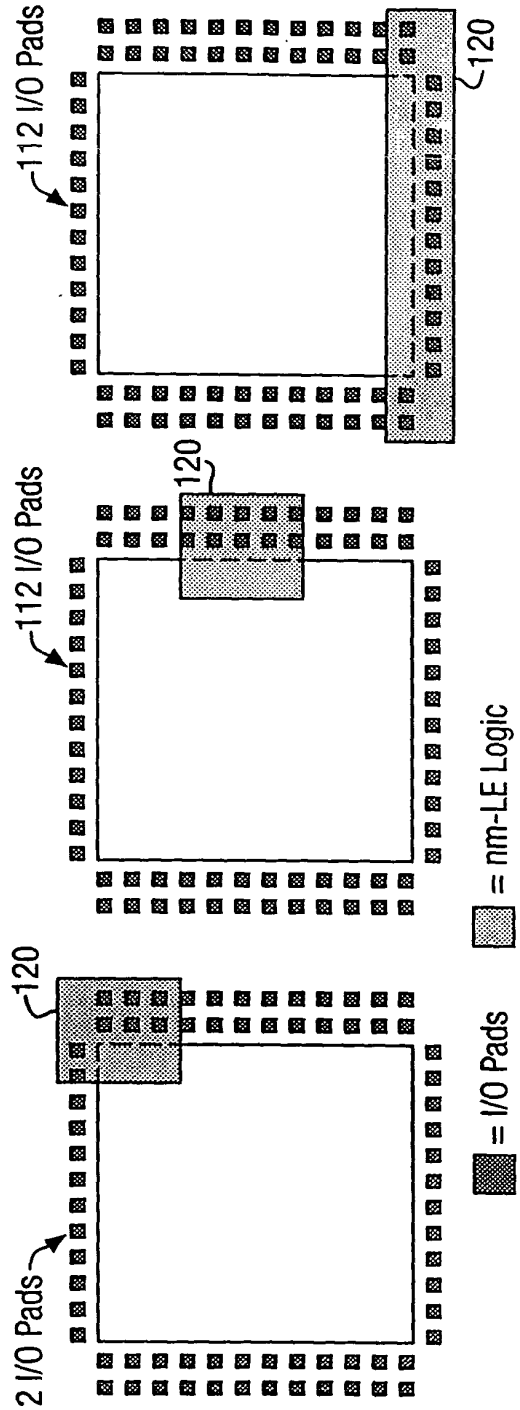

A
B
C
112 I/O Pads
120
= I/O Pads
= nm-LE Logic

Fig. 2.

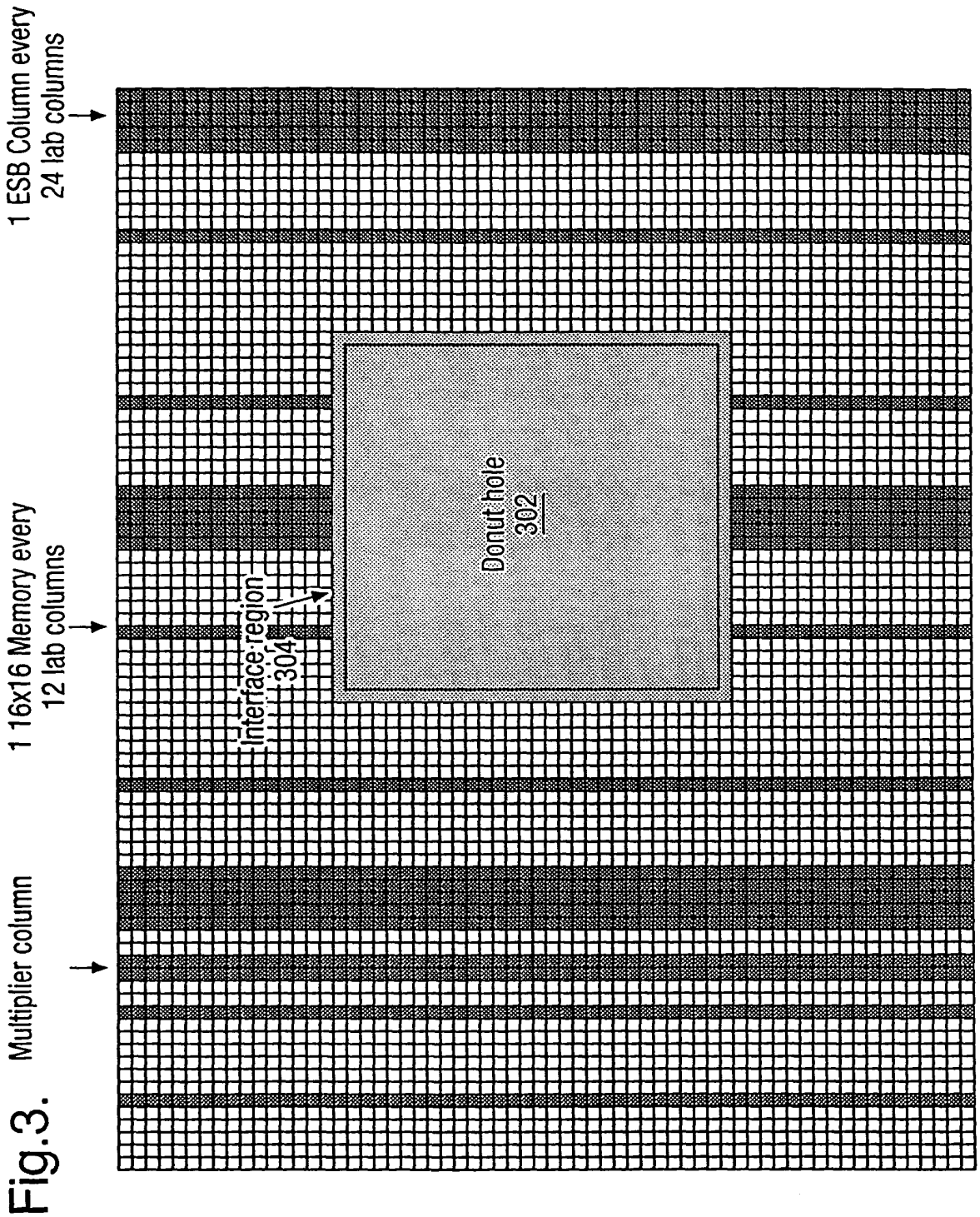

1 ESB Column every
24 lab columns
1 16x16 Memory every
12 lab columns
Multiplier column
Donut hole
302
Interface region
304

Fig.3.

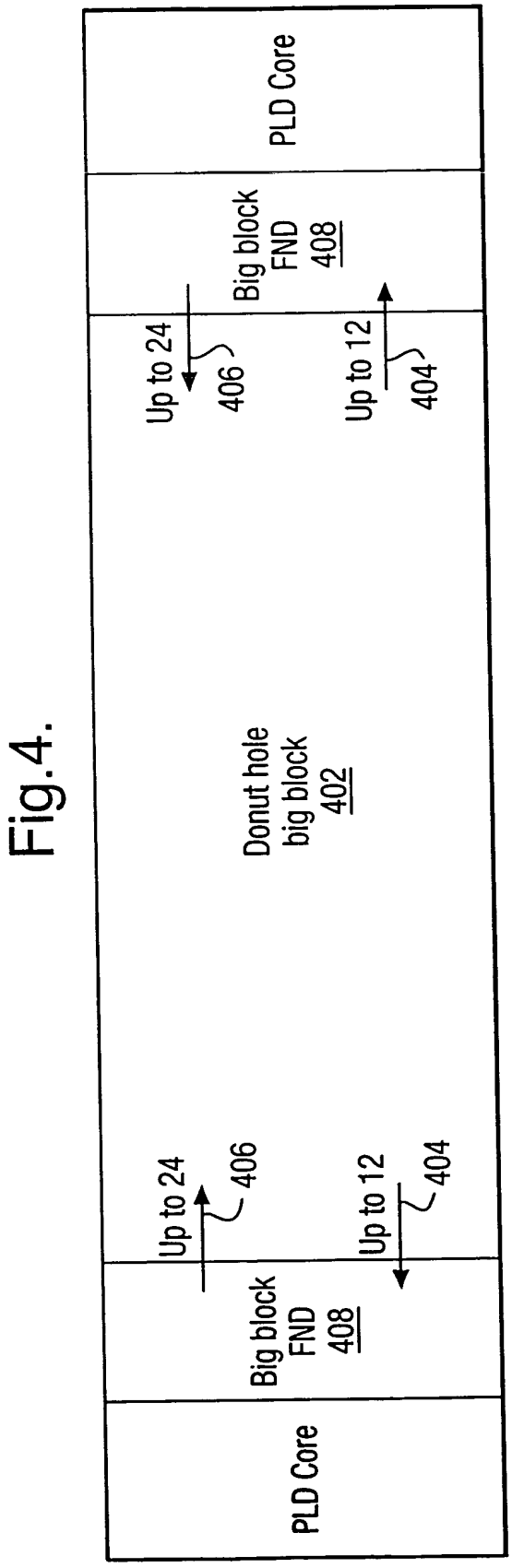

PLD Core
Big block FND 408
Up to 24
406
Up to 12
404
Donut hole big block 402
Up to 24
406
Up to 12
404
Big block FND 408
PLD Core

Fig.4.

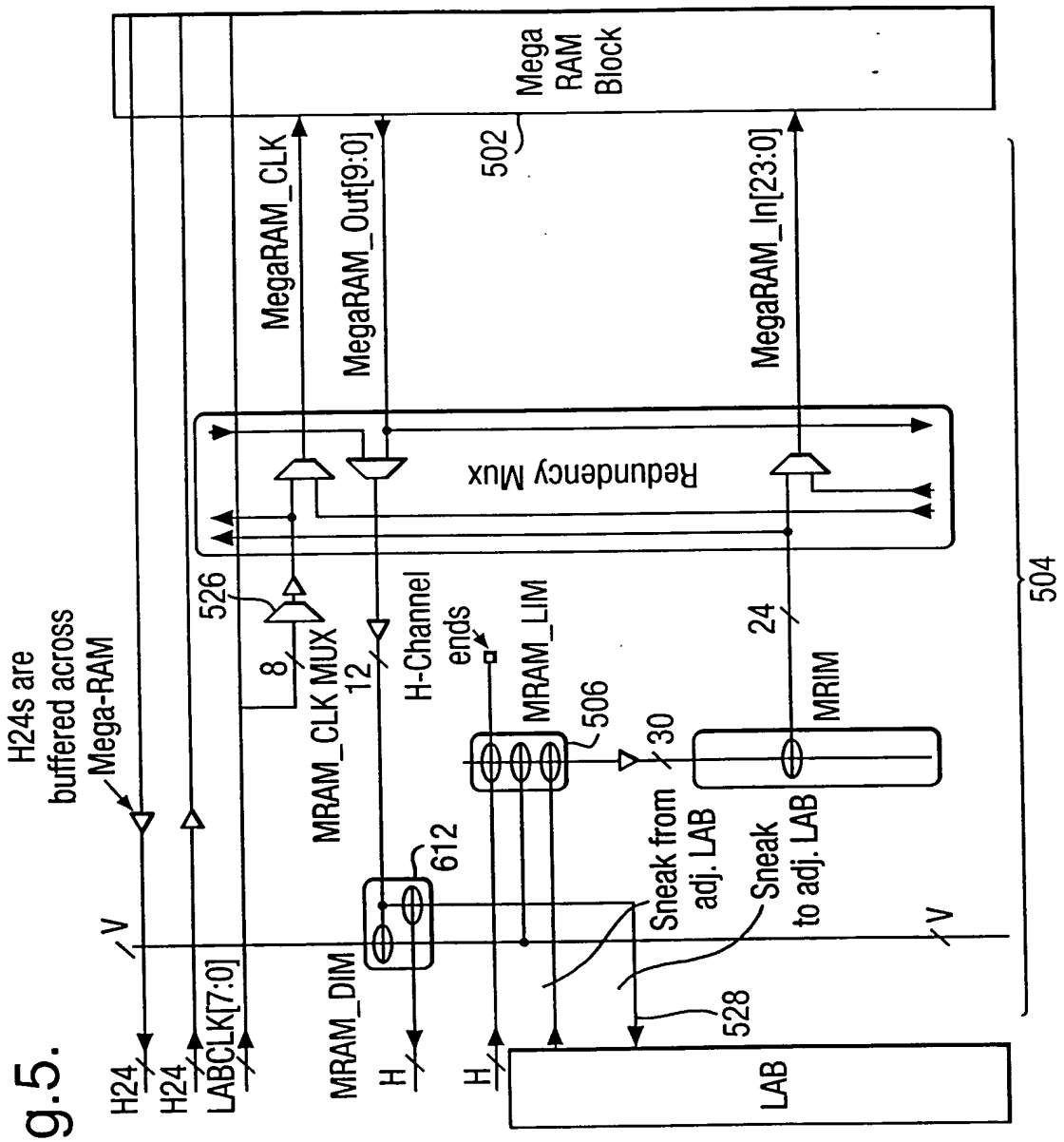

Mega RAM Block
502
MegaRAM_CLK
MegaRAM_Out[9:0]
MegaRAM_In[23:0]
Redundency Mux
504
526
8
MRAM_CLK MUX
12
H-Channel ends
MRAM_LIM
506
24
MRIM
30
612
Sneak from adj. LAB
Sneak to adj. LAB
528
H24s are buffered across Mega-RAM
V
H24
H24
LABCLK[7:0]
MRAM_DIM
H
H
LAB

Fig.5.

Fig.6.

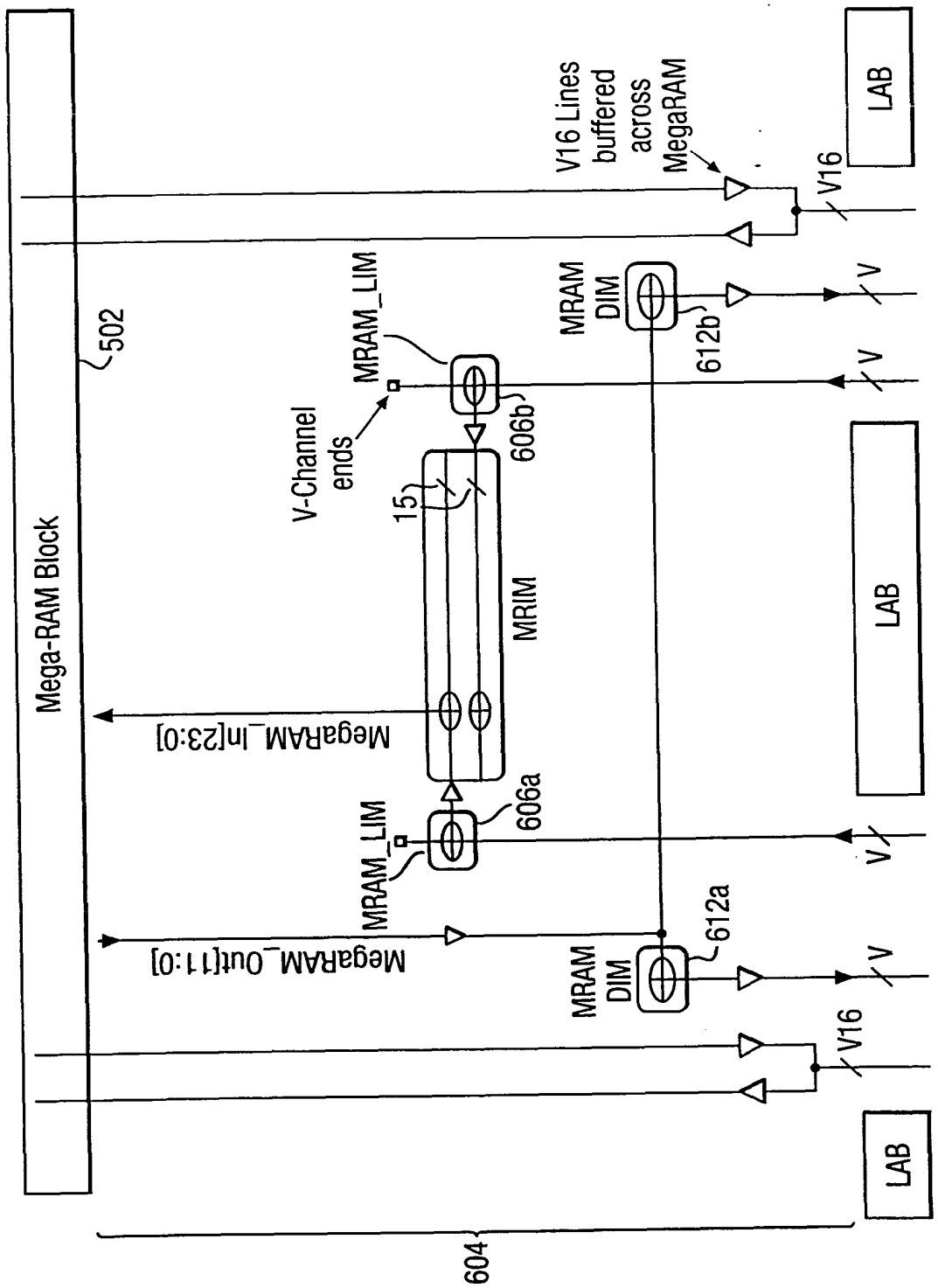

Mega-RAM Block
502
V16 Lines buffered across MegaRAM
LAB
V16
MRAM DIM
612b
V
MRAM_LIM
606b
V-Channel ends
15
MRIM
MegaRAM_In[23:0]
LAB
606a
MRAM_LIM
MegaRAM_Out[11:0]
612a
MRAM DIM
V
V16
LAB
604

Fig.7.

	Horizontal MegaRAM Interface		Vertical MegaRAM Interface	
	Ways in per line	Connections per MRAM_LIM	Ways in per line	Connections per MRAM_LIM
H4	3	8	0	0
H8	3 or 4	2 or 3	0	0
H24	0	0	0	0
V4	1 or 2	4	4 or 5	12
V8	1 or 2	1 or 2	3 or 4	4
V16	0	0	0	0
Sneak path from adjacent LAB	1	0 or 1	0	0
Total MRAM LIM fanin		16		16
Total number MRAM LIM muxes	30		30	

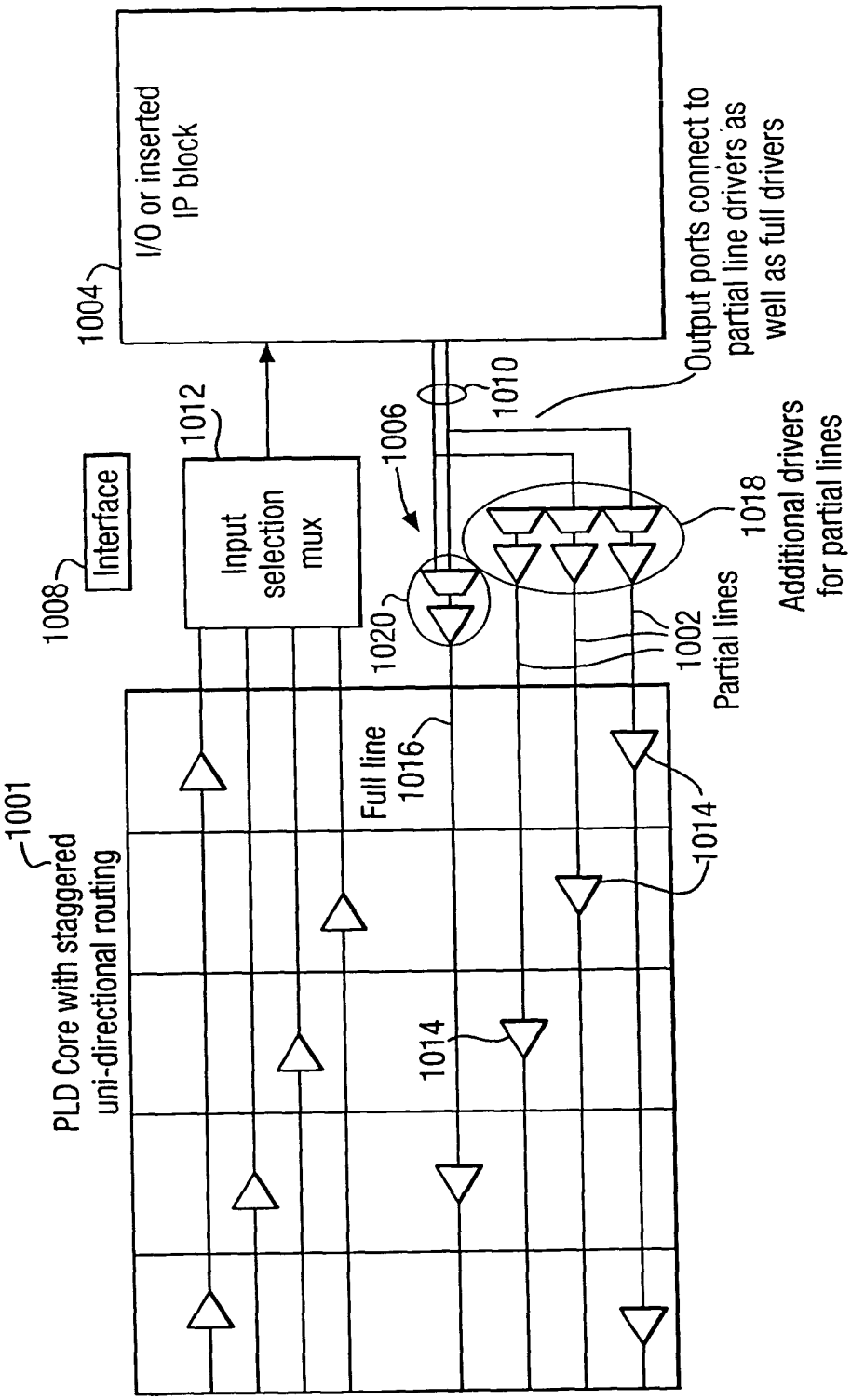
Fig.8.

	Mega-RAM Horizontal Interface	Mega-RAM Vertical Interface
H4 DIM	9 or 10	N/A
H8 DIM	1, 2 or 3	N/A
H24 DIM	0	N/A
V4 DIM	5	5
V8 DIM	2 or 3	1
V16 DIM	0	N/A
Total ways out per MegaRAM Out	17 to 21	6

Fig.9.

	Mega-RAM Horizontal Interface	Mega-RAM Vertical Interface
Lablines	30	30
MRIMs	24	24
H4 Drivers	20	0
H8 Drivers	3	0
H24 Drivers	0 or 1	0
V4 Drivers	10 + 10 redundant	20
V8 Drivers	2 + 2 redundant	4
V16 Drivers	0 or 1 + 0 or 1 redundant	0

Fig.10.


1004
I/O or inserted IP block
1012
1010
Output ports connect to partial line drivers as well as full drivers
1006
1008
Interface
Input selection mux
1018
Additional drivers for partial lines
1020
1002
Partial lines
1001
PLD Core with staggered uni-directional routing
Full line 1016
1014
1014